REMARKS/ARGUMENTS

The office action mailed on July 15, 2011, has been reviewed and carefully considered. Reconsideration is respectfully requested.

Amendments to the Claims

Claims 1, 3, 6 and 7 remain pending in the present application prior to this amendment. Claims 1, 3, 6 and 7 are now pending in the present application; among them, claim 1 is an independent claim. Claim 1 has been amended. The amendments are self-explanatory and do not introduce new matter.

Examiner Interview

On October 11, 2011, the undersigned attorney conducted a series of interviews with the above referenced USPTO examiner.

First, it was agreed that the amendments to the claim overcome the outstanding 35 U.S.C. § 112 rejection.

Second, it was agreed that the amendments to the claim do not expand the scope of the claims.

Third, it was agreed that the arguments below overcome all of the outstanding 35 U.S.C. § 103 rejections.

Because the amendments simply clarify the claimed language and because these amendments do not expand the scope of the claims, then the applicant will maintain the position that the examiner should enter these claim amendments.

Because the arguments overcome all of the outstanding obviousness rejections in the present final office action, then the applicant will maintain the position that the examiner should subsequently issue a notice of allowance.

Nevertheless, the examiner indicated that even though the arguments overcame all of the outstanding obviousness rejections, the examiner stated this did not necessarily mean that an allowance would be forthcoming and that another search would be required.

The applicant recognizes that the examiner may, on his own initiative and time,

perform a brand new search. In the event that this brand new search results in issuing yet another subsequent rejection, then the applicants respectfully remind the examiner that this hypothetical subsequent rejection must be a non-final rejection because it would be based on newly discovered references.

Claim Rejections Under 35 U.S.C. § 112

In the office action (page 2), claims 1, 3, 6 and 7 stand rejected under 35 U.S.C. § 112 as being unclear. In particular, the examiner holds that the recitation "the two flash chips" in claim 1 has no antecedent basis.

The step of partitioning has been amended to read as:

"partitioning physical blocks in the at least two flash chips such that the physical blocks in one of the at least two flash chips have odd logical block addresses and the physical blocks in ~~the other~~ another one of the at least two flash chips have even logical block addresses".

The applicant believes that the defects the examiner indicated have been removed.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 3, 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being obvious over *Ng* (US Patent Application Publication No. 2005/0010717) in view of *Estakhri et al.* (US Patent No. 6081878) for the reasons set forth on Items 4-6 of the Office Action.

Claim 1 has been amended to make the solution of claim 1 more clear. The applicant respectfully submits that the amended claim 1 shall not be obvious over *Ng* in view of *Estakhri et al.* at least for the following reasons.

In the office action, the examiner holds that, "*Ng describes a data write-in method for a flash memory, wherein,..... the method comprises: partitioning physical blocks in the two flash chips such that the physical blocks in one of the chips have odd logical*

block addresses and the physical blocks in the other of the chips have even logical block addresses...". The applicant respectfully disagrees.

***Ng Never Did Disclose the Chip* Interleaving Method**

It is true that *Ng* discloses an interleaving method for accessing flash memory cells using double parallel tracks. However, as recorded in paragraphs [0045] and [0046] as well as Fig. 3 of *Ng*, the blocks in two flash memory cells are partitioned to odd logical block addresses and even logical block addresses. As is well known in the art, a flash chip shall comprise a plurality of blocks, each of which in turn comprises a plurality of pages. As is recorded in paragraph [0045], "the even number of the pages in a block is distributed to the first memory cell, and the odd number of the page in a block is distributed to the second memory cell". That is, it is **the pages rather than the flash chips** (*emphases added*) that have even or addresses in *Ng*.

The examiner's attention is drawn to the fact that the flash memory cells of *Ng* cannot be considered as the physical flash chips of the present application. According to the page interleaving method of *Ng*, the even or odd addresses just refer to the even or odd logical **page** address, not the logical **block** address. More details, according to *Ng*, one chip consists of a plurality of the blocks will have both the even and odd logical page address. In practice, according to *Ng*, when reading or writing on the pages in block0 and block 1 as shown in Figs. 2A-F, the block 0 (mother block) and block1 (child block) will be read or wrote in order of page 0 of block 0 (mother block), page 0 of block1 (child block), page 1 of block 0 and page 1 of block 1.....

To the contrary, according to the present application, the interleaving occurs between the chips and all of blocks in one chip shall have even logical addresses and the blocks in the other chip shall have odd addresses.

***Ng* Gives Contrary Teachings to the Invention**

In addition, as mentioned in the Background of the present application, the problem of the invention is how to improve the operating speed of the flash memory. However, *Ng* provides the contrary teaching.

Specifically, according to the characteristics of flash chip, erase operations have been carried out before writing data to a page. The erase operation can only be performed in a unit of block. Thus, when new data is to being written into the chip, the old data on the target block must firstly be moved /conveyed to another block. Please refer to the Background of the present application for details.

Accordingly, according to *Ng*, when writing data to pages 3 and 4 (for example) of a block, it needs to move the data of pages 1 and 2 and then the data to be wrote will be wrote into pages 3 and 4. In similar way, the data on pages 5, 6, 7....shall be moved accordingly. This block management in combination of the page interleaving method will reduce the speed of operation sharply. Specifically, given a block with 32 pages, in order to carry out the interleaving operation between the pages, it is necessary to bind this block to another block with the same number of pages. That is to say, *Ng* needs to move the data from 64 pages in total, which will reduce the operation speed and increase the risk of the damage of the flash memory.

To the contrary, according the solution as claimed in claim 1 of the present application, physical blocks in the two flash chips are partitioned such that **all** of the physical blocks in one of the chips have odd logical block addresses and **all** of the physical blocks in the another one of the chips have even logical block addresses (*emphases added*). So, during the writing/ reading, the flash chip is selected according to the parity of the logical block address. That is, the reading/writing may be simultaneously carried out between/in at least two flash chips and this operation mode in the two flash chips is different from the page interleaving mode as disclosed in *Ng* and increases the operation speed.

Estakhr et al.Fails Cure the* Defects of *Ng

Estakhr et al. discloses a page interleaving method for accessing the flash memory, which is the same as *Ng* rater than the chip interleaving as the present application. *Estakhr et al* fails to cure the defects of *Ng*. Therefore, it is not easy or obvious for those skilled in the art to incorporate the solution regarding the two chips of *Estakhr et al.* into *Ng* to obtain the solutions as claimed in the amended claim 1 of the present application. Accordingly, claim 1 is not obvious over *Ng* in view of *Estakhr et al.*

In addition, claims 3, 6 and 7 are not obvious over *Ng* in view of *Estakhr et al.*, too, because they depend on claim 1 and recite all the limitations of claim 1. Withdrawal of the rejection of claims 1, 3, 6 and 7 under 35 U.S.C. § 103 is respectfully requested.

Conclusion

For the reasons set forth above, Applicant respectfully submits that claims 1, 3, 6 and 7 pending in this application are in condition for allowance over the cited references. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter.

As a reminder should a new subsequent rejection based on newly cited search be necessitated then this hypothetical subsequent rejection should be a non-final rejection.

This amendment is considered to be responsive to all points raised in the office action. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve those concerns.

Respectfully submitted,

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